



MOS SCRATCH PAD/CONTENT ADDRESSABLE MEMORY SYSTEM

As logic techniques and electronics have evolved, so have memories. The early delay-line memories that had been used only for storage were re-organized into Scratch Pad memories with serial-parallel operational modes, then Content Addressable Memories that permit a search of the memory content for a specific data code. Each organizational change increased the logic power of memory systems. Modern memories can form the basis for small, economical data-manipulation systems that, besides storing data, can gate, group or sequence data, or perform code or format conversion, random-access data search, table look-up and temporary data storage between systems operating at different data rates. A memory with a small amount of peripheral logic is now often a better choice for special purpose data systems than a small computer.

For storage as large as 10,000 bits, a silicon memory can be economically utilized, offering the additional advantages of small size and reliability. It can operate alone in a small electronic system (as in a desk calculator) or as an adjunct to a much larger main memory (for instance, in the computational or peripheral areas of a computer system).

Organization of a Scratch Pad/Content Addressable Memory using currently available MOS products is shown in Figure 1. Figure 2 shows the implementation of one bit of a 64-word memory organized this way. Memory capacity may be expanded by adding storage elements serially to increase the number of words, or by adding the elements shown in parallel to increase the number of bits per word.

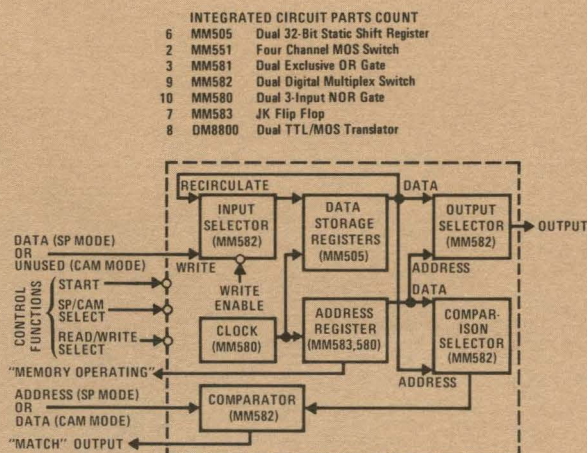


FIGURE 1. Functional Block Diagram of an MOS Scratch Pad/Content Addressable Memory

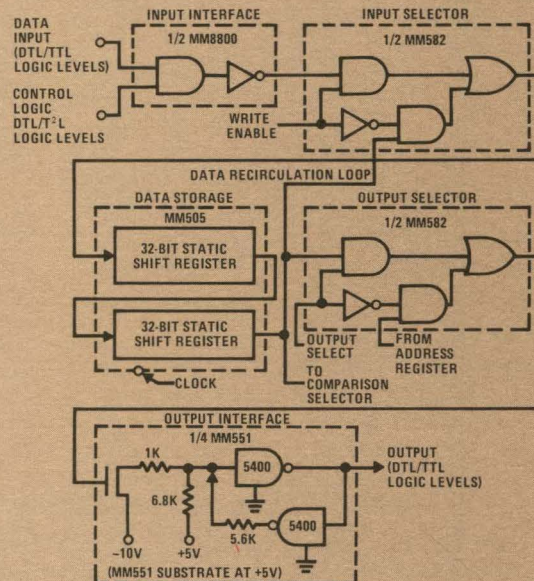


FIGURE 2. Data Flow in a 64-Word Scratch Pad/Content Addressable Memory

All memory operations begin at the first address in memory. The "start" command initiates operation, allowing the clock to sequence the address and memory registers through the possible memory states once. When the sequence is completed, the clock stops and a "memory operating" output is disabled to indicate that the memory is ready for another "start" instruction.

In the Scratch Pad mode, the system outputs the data in the storage registers in parallel. An address presented to the system is compared against the contents of the address register as it sequences through the memory states. The comparison is made by an Exclusive-OR for each bit, with all outputs fed to a NOR gate. When all bits match, a "match" signal stops the clock. If the memory was operating in the read mode, operation is complete and the required data is present at the output. If, instead, new data is to be written into the memory at this address, the comparator output combines with the "write" control signal (Figure 3) to generate a "write enable" signal to the input selector, allowing data present at the input to be transferred into the register.

In the Content Addressable mode, the memory register is searched for a stored word. The normal data input is not used, but instead the required data word is presented to the comparator input. The output selector switches the address lines to the system output, while the comparison selector

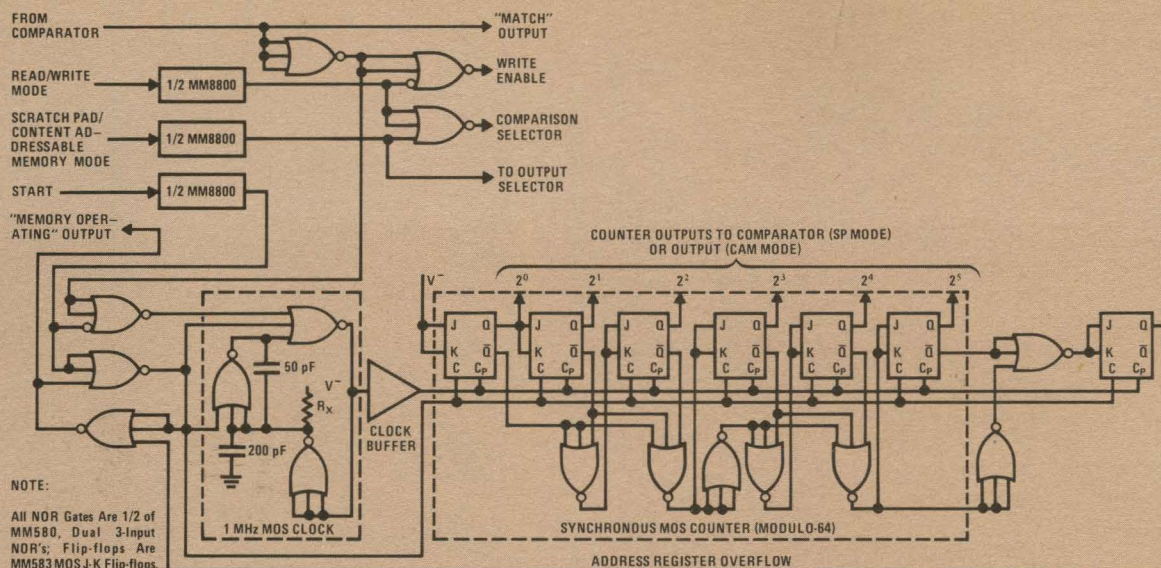


FIGURE 3. Control Logic, Clock and Address Register for 64-Word (6-Bit) MOS Scratch Pad/Content Addressable Memory.

is enabled so the contents of the storage registers are applied to the other side of the comparator.

Operation is similar to that of the memory in the Scratch Pad mode. When there is a match between the contents of the storage registers and the input data word, the clock is stopped and a "match" output is generated. The address of the stored word is now at the output of the memory system. If the word being sought is not stored in memory, the clock will sequence the memory through all its locations once, then stop. This will be indicated by the combinational function of the "Memory operating" line and the "match" line.

When a match is found, the output data remains constant as long as the "start" input remains at a logic "1". When this goes to zero, the clock continues until the address register is again at zero, and the information in the storage register is back at its original location.

An important consideration in the use of this memory system is the interface with bipolar logic circuits. This is readily taken care of on the input by the MM580, a dual voltage translator designed to interface between conventional DTL/TTL voltage levels and MOS devices. On the output side, the circuit in Figure 2 achieves voltage and power translation with good DC margins. The resistor in the feedback produces logic switching with known hysteresis, a necessity when coupling slowly changing logic transitions into high-speed logic elements. Slowly changing inputs applied to a bipolar logic gate can cause the output to oscillate while the input is within the linear threshold region of the

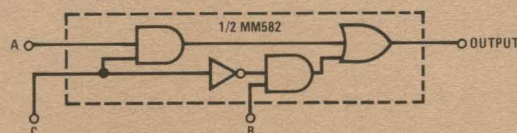


FIGURE 4. The MM582 is a Logic Steering Circuit That Performs the Function of a Single-pole, Double-throw Switch. When the Control Signal C is "True," A Appears at the Output; When it is "False," B Appears at the Output. Operation is Similar in the Input, Output and Comparison Selectors in Memory System.

gate. The hysteresis built into this interface circuit insures a single logic transition at the output of the high-speed detection gate.

A synchronous counter is used in the system (Figure 3) to prevent the possibility of spurious outputs that sometimes occur because of the addition of delayed transients in ripple counters, but the system itself is asynchronous. You can use your own system clock up to 1 MHz or you can tailor the clock shown in Figure 3 for any required rate. Any three inverting gates will oscillate when looped in series. The MM580 is particularly useful in this application because it has a passive pull-up resistor which can be combined with a capacitor for RC network delay timing. In the configuration shown in Figure 3, a logic "1" at the clock input stops the clock. Note also that all unused inputs of an MOS gate must be tied together.

Data sheets and pricing are available for all the MOS elements used in this system.

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